LISTING OF CLAIMS

1. (currently amended) A method for refreshing memory cells, comprising:

determining that a refresh of said memory cells is required;

determining that a data access command has been applied to a command/address bus at a first predetermined time slot~~, said first predetermined time slot being one of a plurality of predetermined time slots defining the only time slots on said command/address bus during which data access commands may be placed on said command/address bus~~ for applying data access commands; ~~and~~

~~initiating said refresh during a time period between said first predetermined time slot and a second predetermined time slot of said plurality of predetermined time slots without delaying said data access~~

determining that said data access command does conflict with said refresh;

completing said conflicting data access;

waiting for a next available time slot upon which said refresh may be initiated;

determining whether a second data access command has been applied to said command/address bus at a second predetermined time slot for applying data access commands; and

initiating said refresh upon reaching said next available time slot and prior to reaching a third predetermined time slot for applying data access commands without conflicting with said second data access.

Claims 2-8 (canceled)

9. (currently amended) The method of claim [[8]] 1 further comprising:

determining that said second data access command does not conflict with said refresh; and

performing said refresh.

10. (currently amended) The method of claim [[8]] 1 further comprising:

determining that said second data access command does conflict with said refresh;

completing said second conflicting data access;

waiting for a next available time slot upon which said refresh may be initiated; and

initiating said refresh upon reaching said next available time slot without conflicting with a third data access.

11. (original) The method of claim 10 further comprising:

satisfying said second data access command by having said data access satisfied with a memory source other than said memory cells such that said memory cells can be refreshed; and

performing said refresh on said memory cells.

12. (original) The method of claim 11, wherein said act of satisfying comprises satisfying said second data access command by having said data access satisfied with a static random access memory cache.

13. (currently amended) A system for refreshing memory cells of a dynamic random access memory (DRAM) comprising:

a memory array containing said memory cells;

a second memory source other than said memory cells;

a communication link for respectively delivering data access commands to said DRAM on a plurality of predetermined time slots, said plurality of predetermined time slots defining the only time slots on said communication link during which said data access commands may be placed on said communication link; and

a controller for operating said memory array in accordance with said data access commands, wherein

said controller is configured to determine that said memory cells require a refresh, [[and]] wherein

said controller is configured to initiate said refresh at a predetermined time and without delaying a data access triggered by a data access command, and wherein

said controller operates said DRAM such that a conflicting data access command is satisfied with said second memory source other than said memory cells and wherein said memory cells may be refreshed.

14. (original) The system of claim 13, wherein said communication link comprises a command/address bus.

Claim 15 (canceled)

16. (currently amended) The system of claim [[15]] 13, wherein said memory source other than said memory cells comprises a static random access memory (SRAM) cache.

17. (original) The system of claim 13, wherein said controller comprises a refresh controller.

18. (original) The system of claim 13 further comprising:

a counter for counting clock cycles of a dynamic random access memory (DRAM) input clock, wherein at least some of said clock cycles define said predetermined time.

19. (original) The system of claim 13, wherein said predetermined time is defined by receiving a predetermined edge of a data access command.

20. (original) The system of claim 19, wherein said predetermined edge is defined as every fourth positive edge of a dynamic random access memory (DRAM) input clock.

21. (original) The system of claim 20, wherein said DRAM input clock has a frequency of approximately 300 MHz.

22. (original) The system of claim 13, wherein said communication link comprises a link for communicating read and/or write commands to said memory array.

23. (currently amended) A memory device, comprising:

a memory controller configured to operate said memory device to:

determine that a refresh of said memory cells is required;

determine that a data access command has been applied to a command/address bus at a first predetermined time slot~~, said first predetermined time slot being one of a plurality of predetermined time slots defining the only time slots on said command/address bus during which data access commands may be placed on said command/address bus~~ for applying data access commands; ~~and~~

~~initiate said refresh during a time period between said first predetermined time slot and a second predetermined time slot of said plurality of predetermined time slots without delaying said data access~~

determine that said data access command does conflict with said refresh;

complete said conflicting data access;

wait for a next available time slot upon which said refresh may be initiated;

determine whether a second data access command has been applied to said command/address bus at a second predetermined time slot for applying data access commands; and

initiate said refresh upon reaching said next available time slot prior to reaching a third predetermined time slot for applying data access commands without conflicting with said second data access.

Claims 24-30 (canceled)

31. (currently amended) The memory device of claim [[30]] 23, wherein said memory controller further operates said memory device to:

determine that said second data access command does not conflict with said refresh; and

perform said refresh.

32. (currently amended) The memory device of claim [[30]] 23, wherein said memory controller further operates said memory device to:

determine that said second data access command does conflict with said refresh;

complete said second conflicting data access;

wait for a next available time slot upon which said refresh may be initiated; and

initiate said refresh upon reaching said next available time slot without conflicting with a third data access.

33. (original) The memory device of claim 32, wherein said memory controller further operates said memory device to:

satisfy said second data access command by having said data access satisfied with a memory source other than said memory cells such that said memory cells can be refreshed; and

perform said refresh on said memory cells.

34. (original) The memory device of claim 33, wherein said memory controller operates said memory device such that said act of satisfying comprises satisfying said second data access command by having said data access satisfied with a static random access memory cache.

35. (currently amended) An integrated circuit semiconductor device containing a system for refreshing memory cells of a dynamic random access memory (DRAM), said integrated circuit semiconductor device comprising:

a memory array containing said memory cells;

a second memory source other than said memory cells;

a communication link for respectively delivering data access commands to said DRAM on a plurality of predetermined time slots, said plurality of predetermined time slots defining the only time slots on said communication link during which said data access commands may be placed on said communication link; and

a controller for operating said memory array in accordance with said data access commands, wherein

said controller is configured to determine that said memory cells require a refresh, [[and]] wherein

said controller is configured to initiate said refresh at a predetermined time and without delaying a data access triggered by a data access command, and wherein

when said controller determines that data stored in at least some of said memory cells is in danger of being lost as a result of not being refreshed, said controller operates said DRAM such that a conflicting data access command is satisfied with said second memory source other than said memory cells and wherein said memory cells may be refreshed.

36. (original) The integrated circuit device of claim 35, wherein said communication link comprises a command/address bus.

Claim 37 (canceled)

38. (currently amended) The integrated circuit device of claim [[37]] 35, wherein said memory source other than said memory cells comprises a static random access memory (SRAM) cache.

39. (original) The integrated circuit device of claim 35, wherein said controller comprises a refresh controller.

40. (original) The integrated circuit device of claim 35, wherein said system further comprises:

a counter for counting clock cycles of a dynamic random access memory (DRAM) input clock, wherein at least some of said clock cycles correspond to said predetermined time.

41. (original) The integrated circuit device of claim 35, wherein said predetermined time is defined by receiving a predetermined edge of a data access command.

42. (original) The integrated circuit device of claim 41, wherein said predetermined edge is defined as every fourth positive edge of a dynamic random access memory (DRAM) input clock.

43. (original) The integrated circuit device of claim 42, wherein said dynamic random access memory (DRAM) input clock has a frequency of approximately 300 MHz.

44. (original) The integrated circuit device of claim 35, wherein said communication link comprises a link for communicating read and/or write commands to said memory array.

45. (currently amended) A processor-based system, comprising:

a processor; and

a dynamic random access memory (DRAM) coupled to said processor, said dynamic random access memory having a system for refreshing memory cells in said dynamic random access memory, said system comprising:

a memory array containing said memory cells;

a second memory source other than said memory cells;

a communication link for respectively delivering data access commands to said DRAM on a plurality of predetermined time slots, said plurality of predetermined time slots defining the only time slots on said communication link during which said data access commands may be placed on said communication link; and

a controller for operating said memory array in accordance with said data access commands, wherein

said controller is configured to determine that said memory cells require a refresh, and ~~wherein~~

said controller is configured to initiate said refresh at a predetermined time and without delaying a data access triggered by a data access command, and wherein

said controller operates said DRAM such that a conflicting data access command is satisfied with said second memory source other than said memory cells and wherein said memory cells may be refreshed.

46. (original) The processor-based system of claim 45, wherein said communication link comprises a command/address bus.

Claim 47 (canceled)

48. (currently amended) The processor-based system of claim [[47]] 45, wherein said memory source other than said memory cells comprises a static random access memory (SRAM) cache.

49. (original) The processor-based system of claim 45, wherein said controller comprises a refresh controller.

50. (original) The processor-based system of claim 45, wherein said system for refreshing memory cells further comprises:

a counter for counting clock cycles of a dynamic random access memory (DRAM) input clock, wherein at least some of said clock cycles define said predetermined time.

51. (original) The processor-based system of claim 45, wherein said predetermined time is defined by receiving a predetermined edge of a data access command.

52. (previously presented) The processor-based system of claim 51, wherein said predetermined edge is defined as every fourth positive edge of a dynamic random access memory (DRAM) input clock.

53. (original) The processor-based system of claim 52, wherein said DRAM input clock has a frequency of approximately 300 MHz.

54. (original) The processor-based system of claim 45, wherein said communication link comprises a link for communicating read and/or write commands to said memory array.

Claims 55-58 (canceled)